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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Revised PTO/SB/30 (08-00)

Attorney Docket No. 32014-150502

RCE $ 0800

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995. See The American Inventors Protection Act of 1999 (AIPA).

Application Number	09/377,740
Filing Date	August 20, 1999
Examiner Name	S. Crane
First Named Inventor	Kimikatsu SHOJI et al.
Group Art Unit	2811
Attorney Docket Number	32014-150502

#17 Req RCE
FJONES 10-30-02

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

NOTE: *37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53 (d) (PTO/SB/29) instead of a RCE to be eligible for* the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Interim Rule, 65 *Fed. Reg.* 14865 (Mar. 20, 2000), 1233 *Off. Gaz. Pat. Office* 47 (Apr. 11, 2000), which established RCE practice.

1. Submission required under 37 C.F.R. § 1.114

   a. ☐ Previously submitted
      i. ☐ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on (Any unentered amendment(s) referred to above will be entered).
      ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on
      iii. ☐ Other

   b. Enclosed
      i. ☒ Amendment/Reply
      ii ☐ Affidavit(s)/Declaration(s)
      iii. ☐ Information Disclosure Statement (IDS)
      iv. ☐ Other

~~Adjustment date: 10/25/2002 SZEWDIE1~~
~~10/24/2002 SZEWDIE1 00000051 09377740~~
~~01 FC:1006 740.00 OP~~

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(i) required)

   b. ☐ Other

3. Fees — The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

   a. ☒ The Director is hereby authorized to charge any deficiency the following fees, or credit any overpayments, to Deposit Account No. 22-0261
      i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)
      ii. ☒ Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)
      iii. ☐ Other

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   b. ☒ Check in the amount of $ 740.00 enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print /Type)	Robert J Frank/ Chad C. Anderson	*Registration No. (Attorney/Agent)*	19,112 and 44,505
Signature	Chad C. Anderson	*Date*	October 23, 2002

VENABLE
P.O. Box 34385
Washington, DC 20043-9998

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01 FC:1801 740.00 OP

SEND Fees and Completed Forms to the following address: Commissioner for Patents, Box RCE, Washington, DC 20231.
PC Docs No. 410216v1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
Kimikatsu SHOJI, et al.	Art Unit: 2811
Appl. No. 09/377,740	Examiner: S. CRANE
Filed: August 20, 1999	Atty. Docket No. 32014-150502
For: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF MANUFACTURING THE SAME	Customer No. 26694 PATENT TRADEMARK OFFICE

18/D
FJOWES
10-30-02

Amendment

Honorable Commissioner for Patents
Box Amendments
Washington, D.C. 20231

Sir:

In reply to the Office Action dated February 27, 2002, Applicants submit the following Amendment and Reply. This Amendment is being filed with a Request for Continued Examination.

No extensions of time or fees for net addition of claims are required. However, if extensions of time are needed to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims), and any other fee deficiency are hereby authorized to be charged, or any overpayments credited, to Deposit Account No. 22-0261.

Amendments

In The Disclosure:

Please amend the disclosure as follows:

Page 1, replace the paragraph beginning on line 27 with the following rewritten paragraph:

The embedded array system in contrast to the above-described gate array system, standard cell system and full custom system has the following characteristics. Namely, according to the embedded array system, dedicated macro cells such as a CPU, a RAM, etc. are embedded in a base array at a design state of an IC layout. In the embedded array system, a layer is provided in which functional elements or devices such as MOS transistors, etc. are formed by using a previously-designed and manufactured mask, and each of the wiring layers for interconnecting the plurality of functional devices with one another is formed over the layer in which the functional elements or devices are formed. Incidentally, each of the wiring layers is normally hereinafter called a "customized layer" because it is designed for each user. On the other hand, the layer in which the functional devices are formed, is hereinafter called a "non-customized layer" because it is used on a general-purpose basis.

Page 6, replace the paragraph beginning on line 26 with the following rewritten paragraph:

In order to previously design and manufacture the common masks for the non-customized layers, the following two conditions must be met. The first condition is as follows: It is necessary to fix patterns for functional elements or devices such as transistors for constituting each non-customized layer and avoid changes in patterns after the design and fabrication of the mask are started. Further, the second condition is as follows: Interconnections in each wiring

layer used as a customized layer are suitably formed in association with the non-customized layer so that desired functions are obtained. Namely, if basic gates (also called "basic cells") based on the gate array system are partially embedded in the IC designed by the standard cell system or full custom system, and the plurality of embedded basic gates are electrically connected to one another and utilized in combination so as to implement the desired functions, then the common masks used for the non-customized layers can be designed and fabricated prior to the formation of the customized layer even in the case of the IC designed by the standard cell system or full custom system.

Page 7, replace the paragraph beginning on line 17 with the following rewritten paragraph:

A process for designing such an IC as to allow the common masks for the non-customized layers to be designed and fabricated prior to the formation of the customized layer, using the standard cell system or full custom system will next be explained.

Page 7, replace the paragraph beginning on line 28 with the following rewritten paragraph:

Next, design resources based on the gate array system are blocked to effect layout design on the area having the potential of change in circuit. The layout of the entire IC is designed while the blocked design resources based on the gate array system are being captured by a CAD (Computer Aided Design) of the standard cell system or full custom system. Upon completion of the layout design of the entire IC, the design and fabrication of the common masks [mask] related to the non-customized layers is started.

Page 8, replace the paragraph beginning on line 8 with the following rewritten paragraph:

Thereafter, when the contents of the circuit is determined in the area having the potential of the change in circuit, each gate array block corresponding to a basic cell block is again laid out using the CAD of the gate array system. The design and fabrication of a circuit mask corresponding to each customized layer are started based on the re-laid out gate array block. Incidentally, the gate array block whose circuit has been determined, is laid-out in a design based on the non-customized layers formed by the previously-designed and fabricated common masks. Namely, the gate array block preceding the determination of the circuit and the gate array block subsequent to the determination of the circuit are respectively made up of the same basic gate comprised of basic gates identical in number in both the vertical and horizontal directions.

Page 10, replace the paragraph beginning on line 4 with the following rewritten paragraph:

Since diffused layers, polysilicon layers, metal wiring layers, etc. are conventionally formed after the design and fabrication of the masks when the IC is designed by the standard cell system or full custom system, it normally took several months to complete the IC. On the other hand, according to the IC chip 1 in an embodiment of the present invention, it is possible to previously design and manufacture the common masks corresponding to the non-customized layers during a logic-simulation stage, for example. Further, the design work such as the logic simulation or the like is continuously performed in parallel with the design and fabrication of the common masks. Thereafter, when the corresponding circuit for the gate array block 34 has been determined, the layout of the gate array block 34 is designed again, and the circuit mask corresponding to a customized layer is designed fabricated.

Page 10, replace the paragraph beginning on line 20 with the following rewritten paragraph:

When the fabrication of the non-customized layers is completed before the start of the fabrication of the customized layer, for example, a TAT required from the start of the fabrication of the customized layer to the completion of formation of all the layers of the IC chip 1 takes the same several weeks as the manufacturing period of the customized layer. Namely, the period from the completion of the design of the IC to the completion of the fabrication of the IC chip can be greatly reduced by several months to several weeks as compared with the prior art in which the IC has been designed using the standard cell system or full custom system.

Page 11, replace the paragraph beginning on line 1 with the following rewritten paragraph:

According to the IC chip 1 related to the embodiment of the present invention, when a circuit change occurs in the gate array block 34, the designer of the IC chip can cope with such a circuit change by redesigning only the gate array block 34 while the contents of the circuit of the non-customized layers is maintained. That is, only the circuit mask related to the gate array block 34 is changed in design. Thus, the circuit change of the gate array block 34 can be completed in a short period of time.